REMARKS

Applicant has amended the claims to clarify the present invention.

Reconsideration and removal of the rejection of Claims 1-20 as obvious under 35 U.S.C. §103(a) in view of a combination of Yamaguchi (U.S. 5,001,533) and Saitoh et al. (U.S. 6,537,369) are respectfully requested in view of the present amendment to the claims and the following remarks.

Significant and unobvious distinctions are present between the present claimed invention and Yamaguchi.

With respect to Claims 1, 3, 5, 7, 9, 11, 13, 14, 16, 17, 19 and 20, Applicant would point out the following.

First, in the present claimed invention, an outgoing base electrode 26 is formed over the first semiconductor layer 14 with an insulation film 18 present therebetween (see FIG. 1 of the present application).

On the other hand, in Yamaguchi, a polycrystalline silicon layer (outgoing base electrode) 26 is not formed over the collector region 31 (see FIG. 3H of Yamaguchi). That is to say, in Yamaguchi, the collector region 31 is formed in an opening 46a formed in a first insulating layer 24, 25, and the polycrystalline silicon layer (outgoing base electrode) 26 is formed on the first insulating layer 24, 25. The Office Action states that a silicon layer 22 of Yamaguchi corresponds to a first semiconductor layer of the present invention. However, this is not correct. The silicon layer 22 of Yamaguchi does not correspond to the first semiconductor layer (collector layer) 14 of the present claimed invention. As described above, in Yamaguchi, a collector layer is illustrated with reference number 31 (see FIG. 3H of Yamaguchi).

Second, in the present claimed invention, a base layer 32 covers a side surface of the outgoing base electrode 26. In the present claimed invention, since the base layer 32 is formed by deposition over the entire surface of the semiconductor substrate 10, and the base layer 32 is patterned by etching after the deposition, it is possible to suppress dispersion of the film thickness of the base layer 32. Therefore, in the present claimed invention, it is possible to stabilize a characteristic of the semiconductor device so that it is possible to obtain high yields.

On the other hand, in Yamaguchi, a base region 32 does not cover a side surface of the polycrystalline silicon layer 26. In Yamaguchi, the base region 32 is grown on the surface of the collector region 31, and the base connecting region 33 is grown on the side surface of the polycrystalline silicon layer 26, respectively, by a selective epitaxial growth method. That is to say, the base region 32 and the base connecting region 33 are formed independently. In Yamaguchi, since the base region 32 is grown by a selective epitaxial growth method (see Col. 6, line 36 to Col. 7, line 3), variation in the thickness of the base region 32 would be large.

Third, in the present invention, the base layer 32 is formed of silicon germanium containing carbon. In the present invention, since the base layer 32 is formed of silicon germanium containing carbon, diffusion of boron out of the base layer 32 can be prevented.

On the other hand, in Yamaguchi, the base region 32 is <u>not</u> formed of silicon germanium containing carbon. In Yamaguchi, the base layer 32 is formed of silicon.

As described above, the present invention is clearly different from Yamaguchi.

Moreover, Saitoh et al. only discloses a semiconductor layer of SiGeC.

With respect to Claims 2, 4, 6, 8, 10, 12, 15 and 18, Applicants would point out the following.

First, in the present claimed invention, a base layer 32a and an outgoing base electrode 26a are formed continuously with each other (see FIG. 9 of the present application). That is to say, the base layer 32a and the outgoing base electrode 26a are formed of one and the same layer. "Continuous" means that the base layer 32a and the outgoing base electrode 26a are formed at the same deposition step. In the present invention, since the base layer 32a and the outgoing base electrode 26a are formed by deposition over the entire surface of the semiconductor substrate 10, and patterned by etching after the deposition, it is possible to suppress dispersion of the film thickness of the base layer 32a. Therefore, in the present claimed invention, it is possible to stabilize a characteristic of the semiconductor device, so that it is possible to obtain high yields.

On the other hand, in Yamaguchi, a base region 32 on the collector region 31, the base connecting region 33 and the polycrystalline silicon layer 26 are <u>not</u> formed continuously with each other. As described above, the base region 32 is grown on the surface of the collector region 31, and the base connecting region 33 is grown on the side surface of the polycrystalline silicon layer 26, respectively, by a selective epitaxial growth method. That is to say, the base region 32, the base connecting region 33 and the polycrystalline silicon layer 26 are formed independently. In Yamaguchi, since the base region 32 is grown by a selective epitaxial growth method, variation in the thickness of the base region 32 would be large, as described above.

Second, in the present claimed invention, the base layer 32 is formed of silicon germanium containing carbon. In the present claimed invention, since the base layer 32 is formed of silicon germanium containing carbon, diffusion of boron out of the base layer 32 can be prevented.

On the other hand, in Yamaguchi, the base region 32 is not formed of silicon germanium containing carbon, as described above. In Yamaguchi, the base layer 32 is formed of silicon.

Saitoh et al. does not cure the deficiencies of the Yamaguchi reference, and merely discloses a semiconductor layer of SiGeC.

As discussed above, the present claimed invention, as presented in Applicant's amended claims, is not taught or suggested in the Yamaguchi reference, alone or in combination with Saitoh et al.

In view of the present amendments to the claims and the above remarks, Applicant's claims are believed to be patentable and early action towards allowance of Claims 1-21 is respectfully requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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